Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **BALANCE**
2. **INPUT-**
3. **INPUT+**
4. **V-**
5. **BALANCE**
6. **OUTPUT**
7. **V+**

**.048”**

**.085”**

**2 1 7**

**3 4 5 6**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .003” X .005” min**

**Backside Potential: V-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .047” X .084” DATE: 11/9/21**

**MFG: MOTOROLA THICKNESS .014” P/N: LF155**

**DG 10.1.2**

#### Rev B, 7/1